

Second-order OTA-C Filters using a Single OTA

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Abstract -A new voltage-mode second-order low pass OTA-C filter is proposed. The filter is integrator-based and uses only one OTA and two grounded capacitors. A multiple-input operational transconductance amplifier (OTA) for the simulation of the proposed filter is also described. The filter has been simulated using a 0.25 μ m CMOS process. The results show that for a cutoff frequency of 50 MHz, the filter dissipates 5.3mW power from a single 2V supply. The dynamic range and RMS noise are 63dB and 91 μ V (up to 100MHz), respectively. Further advantages of the proposed filter are frequency tunability, low sensitivity, low component count and ease of design. A current-mode equivalent of similar features and possibly better performance is also presented.

1. INTRODUCTION

In continuous-time integrated filter designs, filter structures using multiple active devices have been most often used [1]. This has however limited the performance of power consumption and chip size and may not be suitable for application in portable equipment. Recently, active filters using a single active device embedded in a RC network have received some renewed interest, with the active device being the OTA [1], CC [2] and opamp [3] respectively. These filters have achieved low power consumption, small chip area and large dynamic range. In a recent study [4], an integrator-based second-order filter using a single opamp is proposed, which is based on an internally compensated opamp integrator and a passive RC integrator.

In this paper, we propose a second-order integrator-based OTA-C filter which uses a single OTA. This filter is different from the normal single OTA filter in that it is integrator-based and differs from the normal two integrator loop OTA-C type as it needs only one OTA. It is also different from [4] since only active OTA-C integrators are used. The filter has the advantage of low power consumption of single active device filters and low sensitivity of two integrator loop filters.

The paper is divided into the following sections; the proposed filter structures are discussed in Section 2,

simulated results are given in Section 3 and finally some conclusions are presented in Section 4.

2. FILTER STRUCTURE

The proposed structures have several advantages over the conventional second-order filters such as:

1. Compact design with minimum number of components.
2. Only grounded capacitors are used to minimize the parasitic effects.
3. Low power consumption.
4. Low RMS noise and high dynamic range.

2.1 Voltage-mode Filter :

Figure 1 shows the proposed second order low pass OTA-C filter. In the structure the OTA has two pairs of differential input and two outputs with the same current direction.

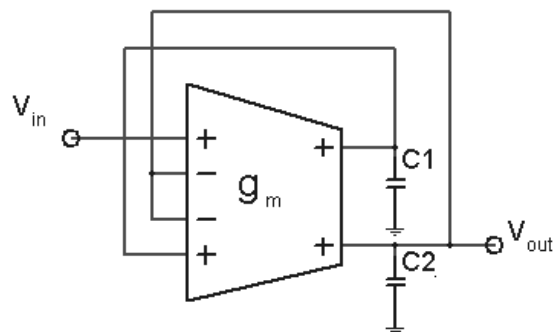


Fig 1 Second-order voltage-mode OTA-C filter using a single multiple-input OTA

Inspection and simple analysis of the architecture show that it is a two-integrator loop filter. The transfer function of the filter can be derived as

$$H(s) = \frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{g_m^2}{C_1 C_2}}{s^2 + \frac{g_m}{C_2} s + \frac{g_m^2}{C_1 C_2}} \quad (1)$$

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The pole frequency ω_0 and the selectivity factor Q are given by

$$\omega_0 = \frac{g_m}{\sqrt{C_1 C_2}} \quad (2)$$

$$Q = \sqrt{\frac{C_2}{C_1}} \quad (3)$$

Q can be accurately implemented in CMOS, due to its dependence only on the ratio of two capacitors. ω_0 can be electronically tuned with g_m since the transconductance is proportional to the bias voltage of the OTA. We may tune the cut-off frequency by using different values of the product $C_1 C_2$. However, in order to maintain the Q of the filter at a constant level the ratio between C_2 and C_1 must remain constant. It can be easily proved that sensitivities of the filter are very low.

The method is more suitable for low- Q design, as large Q may result in large spread in capacitances. Particularly, when $Q=1$, we can have $C_1=C_2=C$, convenient for practical implementation. In this case, ω_0 can be easily controlled by a capacitor array C which can further enhance the tuning range. From equations (2) and (3), design can be easily done. For any chosen value of g_m , C_1 and C_2 can be determined from the equations.

Compared with conventional two integrator loop OTA-C filter designs that use at least two OTAs, the proposed realization in Fig.1 requires only one multiple-input OTA. Compared with traditional single OTA-RC filters containing at least one additional resistor the new structure does not need any resistors. One OTA and two capacitors of the proposed filter are an absolutely minimum number of components needed for a second-order filter. It should thus have reduced power consumption, reduced chip size and increased dynamic range.

2.2 Current-mode Filter:

In analogue circuit design, current-mode techniques are becoming popular because they have many advantages e.g. simplicity of signal operations, low output noise, wide dynamic range, etc, compared with their voltage-mode counterparts.

Similar to the voltage-mode filter proposed, a current-mode equivalent can be constructed, which is

shown in Fig. 2. The current-mode realization in Fig.2 requires only one multiple-output OTA and two grounded capacitors. The OTA can be a normal OTA with two pairs of input and two pairs of output, but with the inverting input terminals being grounded.

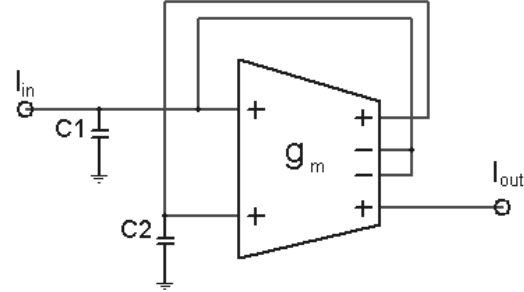


Fig 2 Second-order current-mode OTA-C filter using a single multiple-output OTA

The transfer function of the current-mode filter can be derived as

$$H(s) = \frac{I_{out}(s)}{I_{in}(s)} = \frac{1}{\tau_1 \tau_2 s^2 + \tau_2 s + 1} \quad (4)$$

$$\text{where } \tau_1 = \frac{C_1}{g_m} \text{ and } \tau_2 = \frac{C_2}{g_m}.$$

3. SIMULATION RESULTS

Both voltage-mode and current-mode filters have been simulated using a 2V 0.25um CMOS technology. In the following we give the simulation details of the voltage-mode filter, with a brief discussion of the current-mode one.

3.1 Voltage-mode Results:

The simulation of the voltage-mode filter in Fig. 1 requires a multiple-input OTA with two output currents both flowing out of the OTA. To benefit from its advantages of linearity and tunability [5, 6] we use the cross-coupled type OTA in the filter simulation, shown in Fig. 3. The OTA contains two cross-coupled CMOS transistor pairs, in which one pair is biased with an additional voltage source of low output impedance.

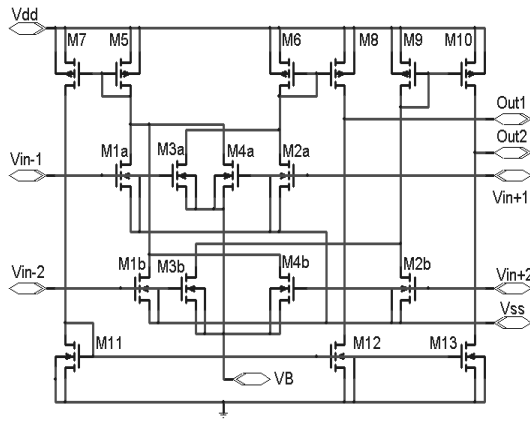


Fig. 3. Transistor-level implementation of multiple input OTA.

The input stage consists of source-coupled transistors pairs M_{1a} – M_{2a} and M_{1b} – M_{2b} and biased source-coupled transistor pairs M_{3a} – M_{4a} and M_{3b} – M_{4b} . Using the standard square-law model for MOS transistors in their saturation region, output current I_{outj} can be expressed as

$$I_{outj} = 2K_n V_a V_{dj} = g_m V_{dj} \quad j=1, 2 \quad (5)$$

where V_{dj} are the differential input voltages, $V_{dj} = V_{in+j} - V_{in-j}$ and $V_a = V_b - V_{ss}$ where V_b is the bias voltage. Equation (5) shows that the transconductance of the proposed OTA is linear and tunable by varying bias voltage V_b .

The OTA-C filter in Fig.1 based on the OTA circuit of Fig.3 was simulated in 0.25 μ m CMOS technology available through MOSIS. Supply voltages $V_{dd}=2V$ and $V_{ss}=0$ were used. SPICE level 7 simulations were performed using the following key model parameters, $V_{tno} = 0.407736V$, $V_{tpo} = -0.587912V$, $K_n = 121.9\mu A/V^2$ and $K_p = 23.2\mu A/V^2$. The multiple-input OTA transistor sizes are given in Table 1.

Table 1 Transistor dimensions

Size um	M1a-M4a M1b-M4b	M5-M10	M11-M13
W	5	5.25	4.25
L	0.25	0.25	0.25

The filter was designed to have a tunable cut-off frequency through g_m and unity quality factor Q , thus $C_1=C_2=C$. The AC response of the filter with $C=5pF$ at different bias voltages is shown in Fig.4 and the details of the cut-off frequency using

different values of load capacitors are shown in Table 2. Obviously, the filter can be coarsely tuned by the discrete capacitor and finely tuned by the continuous bias voltage. It can be noted that the Q of the circuit is slightly higher than expected, due to excess phase in the OTA.

Table 2 Summary of cut-off frequency

Bias Voltage	Capacitor $C_1=C_2$ pF	f_c MHz	Transconductance μS
650mV-1V	5	42-45.5	200-226
650mV-1V	10	21-22.6	200-226
650mV-1V	50	4.2-4.5	200-226

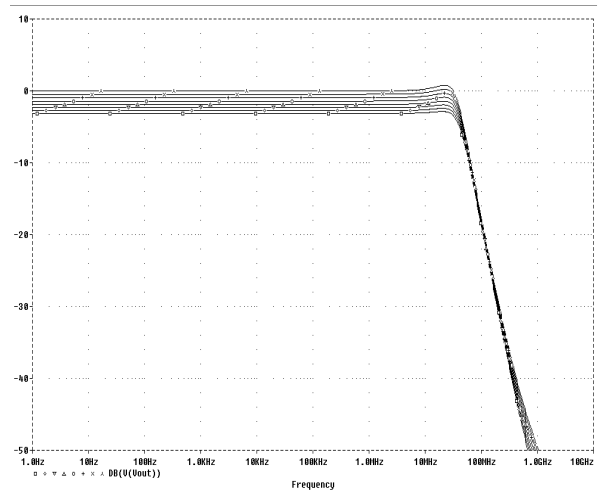


Fig.4. Simulated low pass frequency response (in dB), showing the tuning range

To confirm the theoretical analysis, a 50 MHz filter was designed using an arbitrary value of transconductance. The transconductance was set using bias voltage $V_b=900mV$. The values of capacitors C_1 and C_2 were calculated from Equations (2) and (3). Fig. 5 shows the simulated frequency response of the filter, which is in good agreement with the expected one. Simulations also show that the power consumption of the filter is only 5.3mW, which is low for two pole filters. The dynamic range and RMS noise of the filter are 63dB and 91 μV (up to 100MHz), respectively.

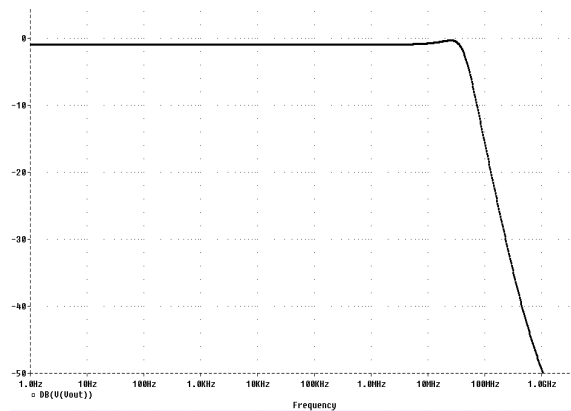


Fig. 5 Magnitude frequency response of the 50MHz filter at the set bias voltage

3.2 Current-mode Results:

The current-mode OTA-C filter in Fig.2 based on the OTA circuit of Fig.3 with some modifications was simulated in PSPICE level 7. The AC response of the filter with $C_1=C_2=5\text{pF}$ at different bias voltages is shown in Fig.6.

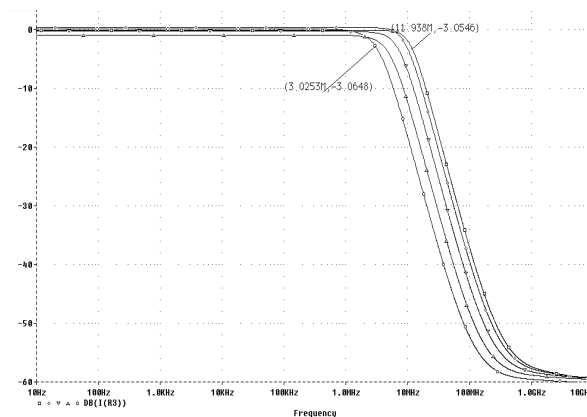


Fig.6 Simulated AC response of the second-order current-mode low-pass filter

The simulated results show that the cut-off frequency of the filter varies from 3MHz to 12MHz with the bias voltage changing from 450mV to 850mV. Simulations also show that the maximum power consumption of the current-mode filter is only 3mW, which is low for a two-pole filter. The dynamic range and RMS noise of the filter are 94dB and $3\mu\text{A}$ (up to 500MHz), respectively. Furthermore, the total harmonic distortion is less than 45dB. These results confirm that the current-mode filter may have wider

dynamic range, less RMS noise and lower THD than the voltage-mode counterpart.

4. CONCLUSIONS

A simple two integrator loop low pass OTA-C filter using a single OTA and two grounded capacitors has been proposed and simulated in 0.25um CMOS technology. Powered with a single supply of 2V the simulated 50MHz filter consumes power of only 5.3mW. The dynamic range and RMS noise are 63dB and $91\mu\text{V}$ (up to 100MHz), respectively. The design idea achieves the minimum number of components for second order filters, one OTA and two capacitors, thus the reduced power consumption, chip area and layout complexity. The parasitic effects are reduced because the filter uses only grounded capacitors. The filter can realize accurate Q due to its dependence on the capacitor ratio only and the cut-off frequency is tunable using a bias voltage. A current-mode counterpart of similar or even better performance has also been presented.

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